

features

- **Complex impedance (R, L, C) measurement**
- **Magnitude and phase measurements of analogue signals**
- **Dielectric behaviour measurement (soil moisture, liquid level, oil ageing, ion concentration, etc.)**
- **4 Differential impedance inputs**
- **3 Single ended analogue inputs**
- **serial-output**
- **On-board oscillator and reset circuitry**
- **On-board synchronous detector**
- **On-board offset and correction of parasitics**
- **Single 5 V supply**
- **High reliability**
- **High phase accuracy, better than 0.1° at 20 MHz**
- **Applications require only few external components**
- **Cascadable for multiple sensor applications**

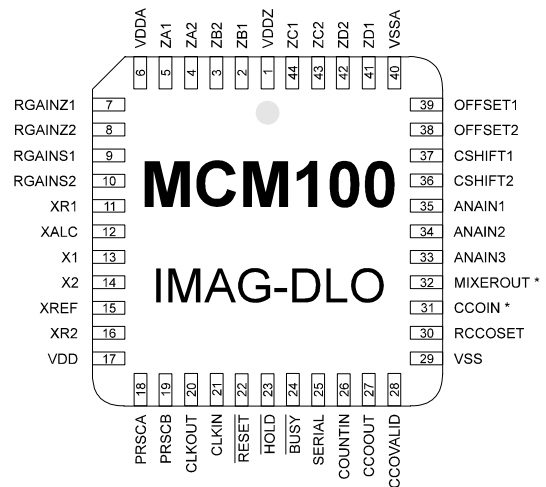


Figure 1. MCM100 Pin configuration.
* not to be used in applications (pin must be left open).

general description

By measuring in all four quadrants of the complex plane, the IC can obtain complex impedance for four input channels at frequencies up to 30 MHz. This makes it for instance suitable to construct (smart) sensors that measure dielectric properties of materials. It was designed for a soil moisture sensor, but it can be used for other measurement applications, such as: liquid level, oil ageing, ion-concentration and electrical conductivity (EC). It can be used for on line measurement of agricultural, environmental and industrial process parameters. It's inputs can directly be connected to electrodes. Many physical parameters are temperature dependant. Therefore the IC has three external analogue inputs. A temperature sensor can be connected to one of them. In this way, the measured values can be corrected for temperature dependency.

To gain the best accuracy, one or two inputs can be used to measure reference components like capacitors and resistors. In this way IC-errors and even internal and external parasitics can be compensated for.

The IC has a serial-output that can directly be connected to a microprocessor device and with a simple RS232-converter to a PC. The baudrate can either be derived from the internal clock oscillator or from an external clock source. It has an output for 22 measuring states, incorporating the 16 states (4x4) for four complex impedance's. In the 6 other states, the output data incorporates the analogue inputs, power supply, internal zero and so on. It has a predefined measuring cycle that can be altered and controlled by an external microprocessor. For multiple sensor applications, several IC's can be cascaded. With only a few external components (a crystal, resistors and capacitors) it can be integrated together with a set of measuring electrodes, then performing all front-end functions, including a connection to a fieldbus or microprocessor for a smart sensor interface.

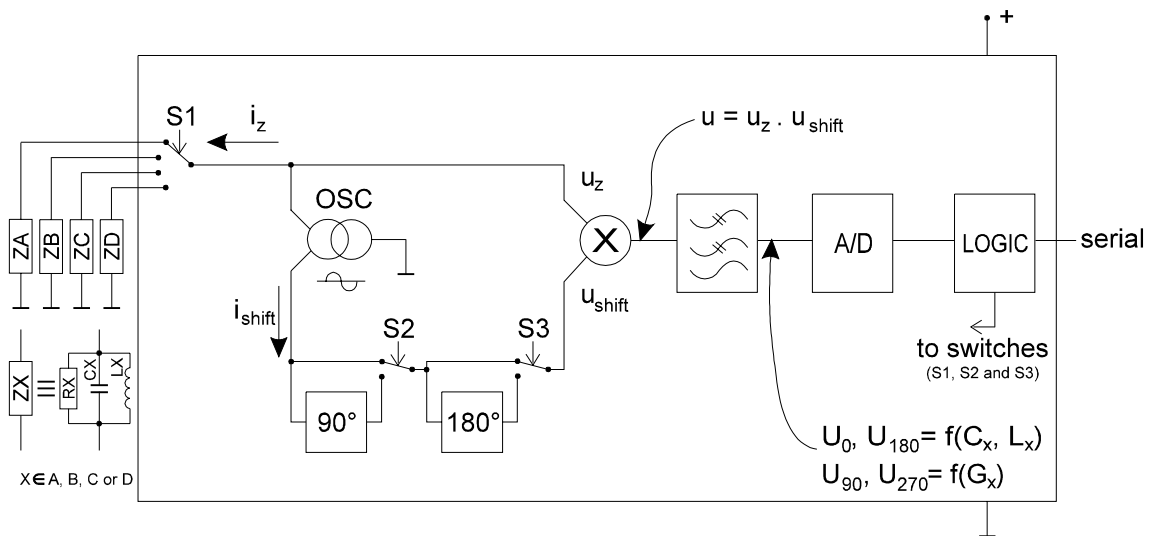


Figure 2. MCM100 Functional block diagram containing a synchronous detector, A/D converter and interfacing and controlling logic. Though the diagram shows the unknown impedances (ZA..ZD) connected single ended, the IC actually has differential inputs.

Figure 2 shows a simplified functional diagram of the MCM100. The IC can measure up to four impedances (ZA, ZB, ZC and ZD). When one or two inputs are connected to references (R, C or L) with exact known values, the internal and external errors (such as offset) can be compensated for. A sine wave current (i_z) with a frequency f_0 from a stabilised oscillator (OSC) develops a voltage (u_z) across the impedances (ZA..ZD) that are successively selected by S1. This voltage is fed to one input of an analogue multiplier. The phase of a second current (i_{shift}) from the oscillator is shifted by respectively 0° , 90° , 180° and 270° . The voltage developed across the phase shifter (u_{shift}) is fed to the other input of the multiplier. The output of the multiplier (u) consists of a DC- and an AC-term with frequency $2\omega_0$. The DC-term (U_{0° , U_{90° , U_{180° and U_{270°) is found at the output of the LPF. In case of a 0° or 180° phase shift, it is a measure (U_{0° , U_{180°) for the capacitance (C_x) or inductance (L_x), and in the case of a 90° or 270° phase shift, it is a measure (U_{90° , U_{270°) for the conductance (G_x) of the unknown impedance (ZX). The output of the low-pass filter is fed to a current-controlled oscillator for analogue-to-digital conversion. Finally the logic converts the digital output to a serial pattern. This serial output is readable for a microprocessor and with an external serial to RS232 level shifter (5 V to ± 12 V conversion) the IC can be connected to a PC.

Remark:
 Whenever in this document is referred to typical it is meant that $f_{Xosc} = 20$ Mhz, $VDD = 5$ V, and no other external components are connected to the IC. $T_{amb} = 25$ °C

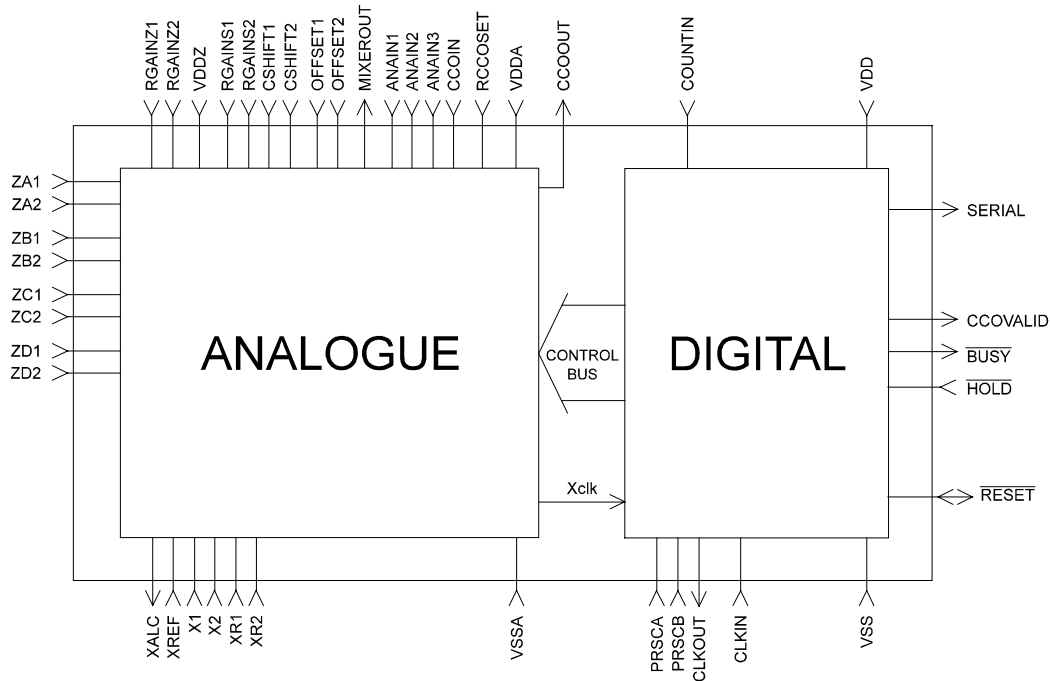


Figure 3. Block diagram of the MCM100. The analogue part is built up with bipolar technology ($f_t = 6 \text{ GHz}$). The digital part consists of CMOS-technology.

Figure 3 shows the block diagram of the MCM100. It is a broad-bandwidth mixed analogue/digital BICMOS integrated circuit that can be used as a **SMART SENSOR INTERFACE (SSI)**. It consists of two parts, a measuring part (analogue) and a controlling part (digital). After power-up the analogue part starts an autonomous, predefined measurement sequence. This sequence consists of 22 states set by the digital part via the control bus. During these states, samples of the four differential impedance inputs (ZA1..ZD2), the three single ended analogue inputs (ANAIN1..ANAIN3), the power supply and the internal offsets are taken for calculation and correction purposes. Data is available from the analogue part as a current (MIXEROUT), or a frequency (CCOOUT). The frequency output can be connected to COUNTIN of the digital part. The digital part generates from this a serial-output signal (SERIAL) for easy interfacing with a microprocessor. The time base for the frequency measurement and the baudrate is controlled with a synchronous clock (CLKIN). This clock can either be derived from an internal prescaler (PRSCA, PRSCB and CLKOUT) or from an external clock source.

The digital part incorporates an internal power on reset and an optional external reset ($\overline{\text{RESET}}$). The operation of the IC can be observed by the CCOVALID line and $\overline{\text{BUSY}}$ line. It's default operation can be altered by the $\overline{\text{HOLD}}$ -line.

To overcome interference problems the digital part (VDD and VSS) and analogue part (VDDZ, VDDA and VSSA) are separately powered.

A digital clock-signal (Xclk) is directly derived from the main clock in the analogue part. This signal feeds the prescaler in the digital part, to form the clock signal (CLKOUT) for the controller circuit.

The control bus contains 10 digital signals controlling the analogue part of the IC (f.i. the switches S1, S2 and S3 from Figure 2). These signals determine the 22 measuring states, as given in Table 2 in the pin description part.

functional description of the analogue part

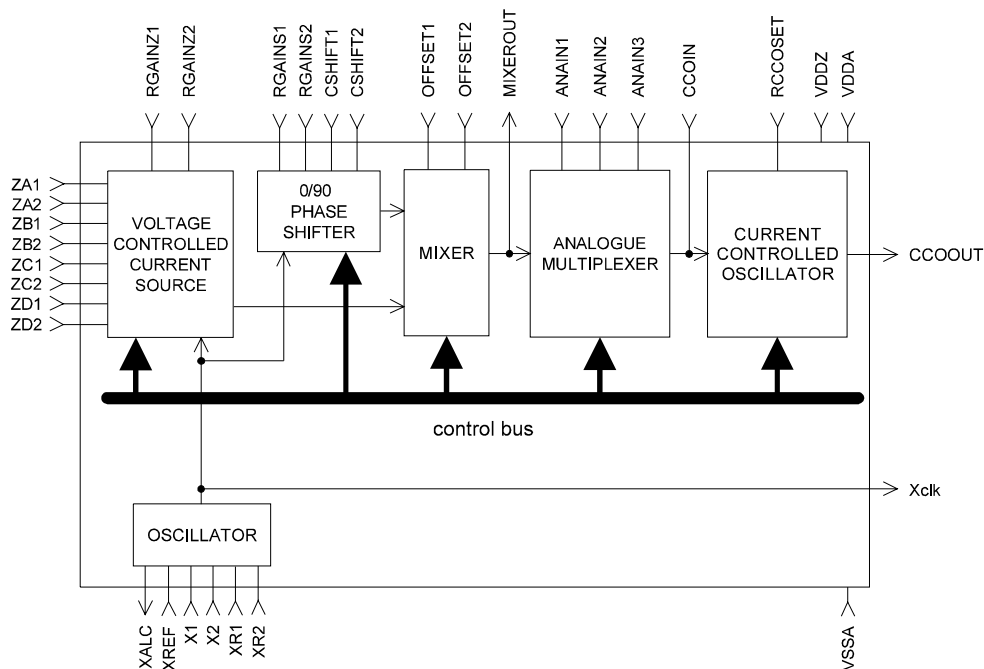


Figure 4. Block-diagram of the MCM100 analogue part.

- The analogue part (of which a block diagram is given in Figure 4) can measure: 4 complex impedance's (R L C) and 3 analogue signals (e.g. temperature).

pin description analogue part

ZA1, ZA2, ZB1, ZB2, ZC1, ZC2, ZD1 and ZD2: The unknown networks are connected across the pins ZA1-ZA2 and so on. For typical applications a reference resistor (100 Ω) and a reference capacitor (100 pF) are connected. These pins generate a balanced alternating sinewave current (typ. 150 μ A eff, 200 mV max.) with reference to VSSA. The voltage, developed due to this current flow through a connected impedance, is measured.

There are no restrictions for the connected impedance (so its range is: 0 - ∞ Ω).

The internal resistance is 644 Ω (\pm 20%) and the internal capacitance is 4 pF (\pm 20%).

RGAINZ1: Gain adjustment resistor+ for Z-channel.

RGAINZ2: Gain adjustment resistor- for Z-channel.

With these pins it is possible to adjust the output current level at the pins ZA1..ZD2.

The adjustment resistor has no restrictions (so its range is: 0 - ∞ Ω). The output current level with no resistor connected ($R = \infty$ Ω) is three times larger than with a 50 Ω resistor connected.

The internal resistance is 483 Ω (\pm 20%).

VDDZ: Analogue power supply input (+5 V for VOLTAGE CONTROLLED CURRENT SOURCE and 90° PHASE SHIFTER circuit).

RGAINS1: Gain adjustment resistor+ for SHIFT channel.

RGAINS2: Gain adjustment resistor- for SHIFT channel.

Used to adjust the signal level in the phase shifter. The adjustment resistor has no restrictions (so its range is: 0 - ∞ Ω).

The internal resistance is 483 Ω (\pm 20%).

CSHIFT1: 90°-Phase shift adjustment point+.

CSHIFT2: 90°-Phase shift adjustment point-.

For optional external phase shift capacitor or resistor. The adjustment resistor has no restrictions (so its range is: 0 - ∞ Ω).

Internal a 660 Ω (\pm 20%) resistance is placed parallel to a 50 pF (\pm 20%) capacitance.

OFFSET1: 0°-Phase shift adjustment point+.

OFFSET2: 0°-Phase shift adjustment point-.

For automatic mixer offset correction via an external amplifier with an offset voltage of 10 μ V.

ANAIN1, ANAIN2 and ANAIN3: Analogue current inputs, single ended.

The maximum input voltage is 4 V.

The internal resistance is 500 Ω .

RCCOSET: Adjustment for CCO output frequency (CCOOUT, typ. 100 kHz at RCCOSET open ($R = \infty$ Ω)). The adjustment resistor has no restrictions (so its range is: 0 - ∞ Ω), however a recommended value for this adjustment resistance is between 100 k Ω - 1 M Ω .

The internal resistance is 73 k Ω (\pm 20%).

VDDA: Analogue power supply input (+5 V).

CCOOUT: CURRENT CONTROLLED OSCILLATOR output.

Measured data is send as a 20 kHz frequency modulating an 100 kHz carrier frequency, with an accuracy of \pm 30%.

This output is an open drain output, therefor the internal resistance has two states (and due to that two values): $R_{\text{open drain}} = 11$ k Ω ; $R_{\text{mosfet on}} = 35$ Ω .

VSSA: Analogue ground.

XR1: Oscillator gain bandwidth control+.

XR2: Oscillator gain bandwidth control-.

The XR1 and XR2 inputs can be used to trim the oscillator gain and bandwidth if necessary.

The XR1 pin may be used for connection of an external TTL-level clock signal via a 10 k Ω external resistor. In this case the frequency is free to choose. For this purpose the crystal must be disconnected from X1 and X2.

A parallel LC resonance circuit between XR1 and XR2 enables to use the oscillator in overtone mode.

X1: To crystal input 1.

X2: To crystal input 2.

There are no restrictions for the crystal, so any frequency desired can be connected.

XREF: Sets ALC (automatic loop control) reference current. Can be used external.

Typical a 10 k Ω resistance is single ended connected. If this resistor is connected to ground, this will cause the output current at ZA1..ZD2 to increase. However if the resistor is connected to VSS, this will cause the output current at ZA1..ZD2 to decrease.

XALC: Oscillator automatic loop control voltage. Can be used external.

This pin can be used to switch the oscillator on (XALC open, no connection) or off (XALC connected to VDDA).

detailed description of the analogue part

The analogue part contains six blocks that will be described in this section (see Figure 4).

VOLTAGE CONTROLLED CURRENT SOURCE: This circuit applies an RF differential current signal to the network under test and passes the voltage developed ($U = I * Z$) to the MIXER. The input is a common base stage to prevent miller feedback. The input circuit is fed by the output of the OSCILLATOR. The current level can be lowered by connecting an external resistor between RGAINZ1 and RGAINZ2. With a resistor of 50 Ω , the current is approximately lowered by a factor of three. Channels not used are de-biased, their pins will go to a high-impedance state. The

circuitry of the channels switched on will not affect the circuitry of the switched off channels. The output level, when de-selected, is less than -80 dB with respect of the signal in active state, if all channels are loaded with 100 Ω .

PHASE SHIFTER: The PHASE SHIFTER generates a reference signal for the mixer. This signal is 0° and 90° shifted with respect of the inputs of the VOLTAGE CONTROLLED CURRENT SOURCE circuit. With the CSHIFT pins, phase can be adjusted.

The internal load on the 0° shift channel is 160 Ω // 2 pF and the internal load on the 90° shift channel is 1920 Ω // 50 pF.

The actual phase shift for 0°-shift is $2.3^\circ \pm 2^\circ$ and the actual phase shift for 90°-shift is $85^\circ \pm 2^\circ$.

The DC voltage at the input pins is 3.5 V (typ.) and the AC voltage across the input pins is 150 mV (p.p.).

The output is a differential current sink that feeds the reference input of the mixer. The output current level is 1 mA-DC, modulated with $\pm 200 \mu\text{A}$.

MIXER: The MIXER is used to determine the magnitude of the voltage from the VOLTAGE CONTROLLED CURRENT SOURCE relative to the phase of the reference signal from the PHASE SHIFTER. The MIXER is of the double balanced type. The reference input may be used either completely or linear driven. An input reference of less than 0.2 mA AC will drive the input linear, this the typical case. The output of the MIXER is a single ended DC current that is switched to the CCO by an ANALOGUE MULTIPLEXER.

ANALOGUE MULTIPLEXER: The ANALOGUE MULTIPLEXER switches the CURRENT CONTROLLED OSCILLATOR from the Z-input or one of the three external analogue inputs (ANAIN1, ANAIN2 and ANAIN3) to the CURRENT CONTROLLED OSCILLATOR and an external pin CCOIN.

CURRENT CONTROLLED OSCILLATOR: The input of the CURRENT CONTROLLED OSCILLATOR is a current of typical $\pm 100 \mu\text{A}$. The input voltage is fixed to 4 V DC. The output of the CURRENT CONTROLLED OSCILLATOR is information that is send as a 10 kHz frequency superimposed on an 100 kHz (typ.) carrier frequency, with an accuracy of $\pm 30\%$. The output frequency and the modulation depth of the CURRENT CONTROLLED OSCILLATOR can be adjusted with the external resistors RCCOSET and/or a resistor from CCOIN to VDDA or VSSA. The bandwidth of the CURRENT CONTROLLED OSCILLATOR is small and is used as an LPF for the MIXER output. If necessary an additional LPF may be formed by connecting a capacitor in parallel with RCCOSET. The output is an N-CMOS transistor with a resistance less than 25 Ω , it can drive directly a coax cable with correct termination to the VDD.

OSCILLATOR: This is a sine wave oscillator that can be used with a crystal or a series LC resonance circuit. It is fully balanced and has a minimum effect on VDD. The output is regulated in order to keep the harmonics as small as possible.

The frequency has a range from 10 MHz up to 30 MHz, with a nominal of 19.6608 MHz. This block has differential analogue current outputs of 1 mA peak-peak $\pm 20\%$. The frequency stability is $\pm 0.1\%$ and the amplitude stability is $\pm 1\%$. The odd harmonics are less than 40 dB. The output current level is set by the resistors RGAINZ for the Z-input circuit (VOLTAGE CONTROLLED CURRENT SOURCE) and RGAINS for the PHASE SHIFTER circuitry. The typical values for these resistors are RGAINZ = 50 Ω and RGAINS = "open". The amplitude of the OSCILLATOR is controlled with an automatic loop control that can be overruled by an external control voltage (0 - 5 V) by means of pin XALC. This pin can also be used to decouple the ripple on the ALC signal if necessary.

functional description of the digital part

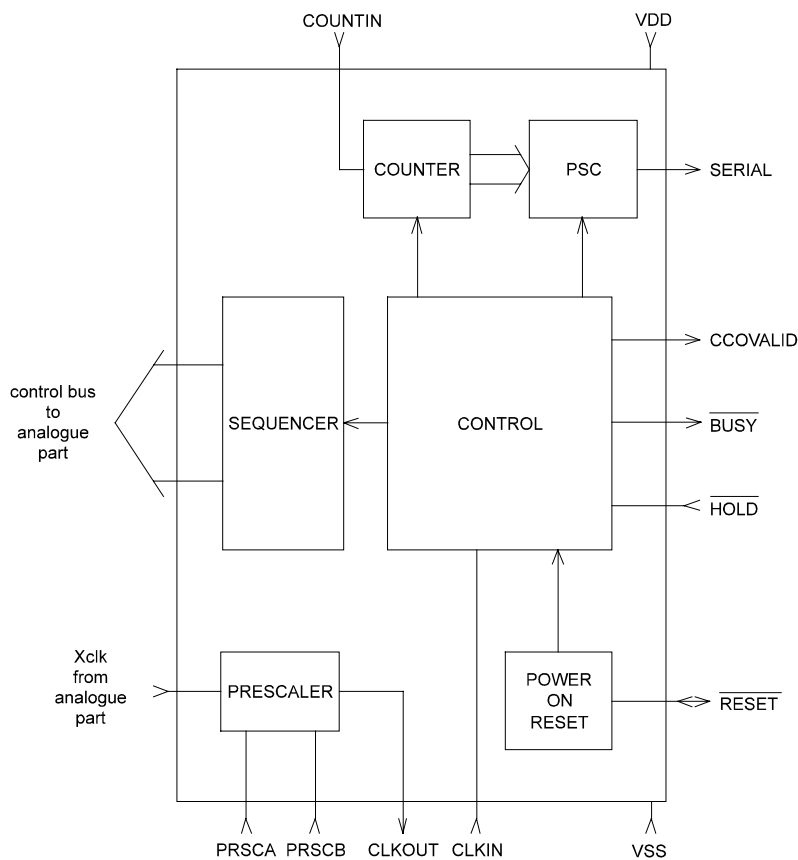


Figure 5. Block-diagram of the MCM100 digital part.

- The digital part (of which a block diagram is given in Figure 5) controls the analogue part via the control bus. There are 22 possible measurement states. The duration of every state is dependant on the clock frequency (CLKIN). Every state consists of 122 clock cycles.
- The digital part measures frequencies (COUNTIN) and gives the result in a digit BCD-format (SERIAL) for every state.
- The digital part contains a prescaler that can be used to derive a low frequency system clock (CLKOUT) for the digital part (CLKIN) from the analogue high frequency crystal clock (Xclk). PRSCA and PRSCB set-up the division factor for the prescaler.
- The process of stepping through the states can be stopped and started at a state with the $\overline{\text{HOLD}}$ -input.
- The output CCOVALID indicates when a measurement is valid.
- The $\overline{\text{BUSY}}$ -signal indicates the moments when measurements (internal or external) are being taken.
- The digital part contains two reset facilities. An internal power-on reset and an external reset input ($\overline{\text{RESET}}$).

Table 1 gives the digital pin characteristics. More about the pin characteristics is given in the pin description section.

name	type	pin	compatibility	comments	Active level
VDD	power	17	+5 V	digital power supply	(H)
PRSCA	input	18	CMOS	Static operation	L or H
PRSCB	input	19	CMOS	Static operation	L or H
CLKOUT	output	20	CMOS	$f_{max} = 2$ MHz	clock
CLKIN	input	21	CMOS	$f_{max} = 2$ MHz	clock
RESET	input output	22	CMOS	Schmitt-trigger/pull-up low level during power on reset	L
HOLD	input	23	CMOS	asynchronous, internally clocked	L
BUSY	output	24	CMOS	synchronous	H
SERIAL	output	25	CMOS	start bit = high (inverted logic)	H
COUNTIN	input	26	CMOS	$f_{max} = 1$ MHz (asynchronous)	clock
CCOOUT	output	27	Open-drain	internal pull-up, $R_{CCOOUT} = 11k2$ Ω	L
CCOVALID	output	28	CMOS	synchronous	H
VSS	power	29	0 V	digital ground	(L)

Table 1. Digital pin-characteristics.

Pin description digital part

VDD: This is the positive power pin for the digital part.
 In the application special care must be taken to decouple this line from the analogue power VDDA.
 The typical supply voltage must be $+5V \pm 10\%$.

COUNTIN: Input for counter.
 This is a standard CMOS input pin. It can be connected directly (externally) to the CCOOUT-pin from the current controlled oscillator of the analogue section. It is also possible to connect an other external device to measure frequency. COUNTIN is coupled to an internal 5-decade COUNTER. The maximum frequency that can be measured is 1 MHz. The input is asynchronous with the system clock (CLKIN). It is internally gated.

PRSCA and PRSCB: Inputs to set the prescaler output frequency.
 With these two digital inputs the prescaler factor can be set to 16, 512, 1024 and 2048 (typ.). With an Xclk-frequency of 20 MHz and a factor of 2048, a clock-frequency (CLKOUT) of 1220 Hz (baudrate SERIAL-output) will be generated, and a state time of 100 ms (see also Table 3).

CLKOUT: Clock-output from the PRESCALER.
 At this pin a square-wave clock signal is available that can drive the CLKIN-pin as a system clock for the digital part. The maximum frequency at this output is 2 MHz with $f_{Xclk} = 32$ MHz and a prescaler dividing factor of 16.

CLKIN: System clock-input to drive all the digital part.
 All actions in the digital part are synchronised to this clock. Typical operating frequency: 1220 Hz. This clock-input can be connected to the output of the prescaler (CLKOUT) or to an external clock source. It's frequency is direct related to the baud rate of the SERIAL-output.

VSS: This is the digital ground.
 This ground is internally de-coupled from VSSA (analogue ground).

RESET : The reset-input for the digital part.
 Internally a pull-up resistance is connected to this input. The input gate has some hysteresis so with an external capacitor, a defined reset time can be generated (with $C_{reset} = 100$ nF, $t_{reset} \approx 10$ ms). The IC is reset and stopped with a low level and starts with a high level on this input. The reset must be held low for at least 3 system clock cycles before it will operate.
 A cold power on reset can be generated by the internal power on reset-circuit (POR). During a cold power on reset the reset-pin will be an output that is held low. In this way an external capacitance is clamped to zero and uncharged until the POR is ready. For testing purposes a cold power-up

can be generated by holding the $\overline{\text{HOLD}}$ -line low during a reset, for at least three clock cycles. This emulates the internal POR function (see power on reset timing diagram, figure ...).

HOLD : Input line to stop the normal state sequence.

With the $\overline{\text{HOLD}}$ -input held high, the IC will operate normally and the sequence repeats its sequence after the 22nd state. A low on the $\overline{\text{HOLD}}$ -input will stop the sequencer at the current state. The measuring of the corresponding parameter continues and every state time a new result is put out at the SERIAL-line. A positive edge on the $\overline{\text{HOLD}}$ -input triggers the sequencer to start a new state. With quick pulses on this input it is possible to step through the sequencer rapidly and stop at a certain state. The $\overline{\text{HOLD}}$ -line must be held low for at least two system clock-cycles to skip states (see $\overline{\text{HOLD}}$ -timing diagram, figure ...).

BUSY : Output-pin.

This line is high during the period that the internal analogue part is actually measuring. This line is low during a reset and at the time that an external analogue input can be measured. It can also be used for external synchronisation purposes. When this line is externally connected to the $\overline{\text{HOLD}}$ -input the circuit will only generate one sequence of states and stops at state 23, each time a power is supplied to it (see functional timing diagram, figure ...).

CCOVALID: Output from digital part.

This is an output that indicates when the IC is actually measuring and when it changes state. This pin can be used for external synchronisation purposes. This line is low during state transitions and during state S0 and S23 (see functional timing diagram, figure ...).

SERIAL: Serial output-pin.

The IC outputs its state information through the SERIAL-pin. During every state the IC outputs a 6 byte serial ASCII pattern that reflects the total count of the COUNTIN-pin, including the state number. Measurement and output of data are pipe-lined internally, so during state n, the measurement of state n-1 is outputted. The serial pattern contains 1 start bit, 7 data bits and 1 stop bit for each character. No parity is used. Every sequence contains 132 characters (22x6) embedded in-between two extra characters indicating the beginning (@) and ending (↔) of a packet. The start bit is active high. The SERIAL-pin is normally low. The serial data is sent in packages that start with an @ followed by the states A, B, ..., U, V and is ended with an ↔. Every state is followed by a decimal value that is in the range of 0 to 99999. E.g. typical output package could look like: @A09976B10952....V10047↔@A10723

The MCM100 keeps sending these data packages as long as it is powered. The contents of a package and the sequence of the states are shown in Table 2. Data values are relative, there is a linear relation with the actual measured values.

state number	decimal value	ASCII character	state name	comments	
start	64	@	POWER UP	no measurement	
01	65	A	ANAIN3	analogue input 3	
02	66	B	ZERO1	offset before measurement	
03	67	C	ANAIN1	analogue input 1	
04	68	D	ZA0°	input A quadrant 1	
05	69	E	ZA180°		quadrant 3
06	70	F	ZA90°		quadrant 2
07	71	G	ZA270°		quadrant 4
08	72	H	ZB0°	input B quadrant 1	
09	73	I	ZB180°		quadrant 3
10	74	J	ZB90°		quadrant 2
11	75	K	ZB270°		quadrant 4
12	76	L	ZC0°	input C quadrant 1	
13	77	M	ZC180°		quadrant 3
14	78	N	ZC90°		quadrant 2
15	79	O	ZC270°		quadrant 4
16	80	P	ZD0°	input D quadrant 1	
17	81	Q	ZD180°		quadrant 3
18	82	R	ZD90°		quadrant 2
19	83	S	ZD270°		quadrant 4
20	84	T	ANAIN2	analogue input 2	
21	85	U	ZERO2	offset after measurement	
22	86	V	ANAIN3	analogue input 3 *	
stop	29	↔	DISABLE	no measurement	

* ANAIN3 can be used as a temperature channel, as it can be measured before and after a total measurement cycle

Table 2. State overview.

calculation of impedance and analogue inputs

detailed description of the digital part

The digital part contains six blocks that will be described in this section (see Figure 5).

COUNTER: The COUNTER is a 5 digit BCD-counter with a gate, clear and reset, that counts pulses from the COUNTIN input. When the state time is 100 ms (typ.) and the frequency from the CCO is 100 kHz with a modulation of 10% , the normal count-range will be 9000-11000 counts. Its output is available for the serial converter through a bus. At the beginning of every state the counter is cleared by the CONTROL block.

PSC: The PSC (PARALLEL-TO-SERIAL-CONVERTER) transforms 20 bit (5x4 bit) parallel information from the COUNTER and the state number from the SEQUENCER, into a serial pattern at the SERIAL-output, in an ASCII-format. Special characters are added to the total packet (22x6 bytes) to mark the begin(@) and end(↔) of the packet. In that way a microprocessor can separate data from two successive measurement cycles. There are no parity check or block check characters added to the packet. When a measurement is not completed, for instance by generating a HOLD, the serial converter will not give an output.

SEQUENCER: The SEQUENCER has 24 states and it controls the analogue part. During every state the analogue section can measure a certain parameter. The SEQUENCER increments its states at command by the CONTROL-BLOCK.

CONTROL: The CONTROL-block contains reset circuitry and logic to perform the HOLD and RUN function. From the RESET-input and the analogue Power-on reset, this block generates an internal

reset that is synchronised to the digital clock (CLKIN). With this reset the digital part of the IC is reset, except for the PRESCALER.

PRESCALER: The PRESCALER divides the high frequency analogue clock Xclk down to a system clock with lower frequency (CLKOUT) for the digital section. This output can directly be connected to the digital clock input CLKIN, through which the complete digital part is synchronously clocked (Alternatively an external clock source can be used for CLKIN). The default dividing factor of the prescaler is 2^{14} . Three other dividing factors are possible by setting the multiplexer with the two digital inputs: PRSCA and PRSCB. Because the IC has a pipe-lined data path without memory capacity, to avoid serial-overflow, the baud rate generator and the timer are tightly coupled and their timing is directly related to the frequency of the system clock (CLKIN). The duration of the states is typical 100 ms and the baud rate of the serial output is typical 1220 Bd. In Table 3 an overview is given for all the settings of PRSCA and PRSCB. With PRSCA and PRSCB both high, a high frequency output is generated to drive an external divider.

PRSCB	PRSCA	standardised Baud rate ($\pm 1,7\%$)	f_{CLKOUT} (Hz)	State time (ms)
0	0	1200 Bd.	1220	100
0	1	2400 Bd.	2440	50
1	0	4800 Bd.	4880	25
1	1	for external generator	1.25 MHz	97.6 μ s

Table 3. Timing and baud rate related to the clock frequency ($f_{Xclk} = 20$ MHz, typ.).

POWER ON RESET: The reset for the prescaler is directly derived from the internal power-on-reset. The external reset (\overline{RESET}) is clocked and cannot be used for the prescaler in the application because otherwise a hang-up would occur during start-up. For test purposes it is possible to reset the prescaler by holding \overline{RESET} and \overline{HOLD} low for at least 3 system clock-cycles as this emulates a cold power-on. The prescaler is build-up as a ripple counter, to avoid high frequency spikes on the power lines and to reduce power consumption. The IC comes in at 4.4 V and falls off at 4.1 V. Its operating voltage is 5 V.

timing definition

The timing for the digital part is defined for typical: $V_{DD} = 5$ V and $T_{amb.} = 25$ °C, worst case: $V_{dd} = 4.5$ V and $T_{amb.} = 75$ °C and best case: $V_{dd} = 5.5$ V and $T_{amb.} = -10$ °C, all with an external load of: $C_{load} = 125$ pF at the CMOS outputs of the circuit. Timing is defined with a system-clock frequency of $f_{CLKIN} = 1.25$ MHz. This frequency is typical the prescaler has a first stage divider factor of 16, and with $f_{Xclk} = 20$ MHz. Figure 6 gives the timing diagram and Table 4 gives the timing definition.

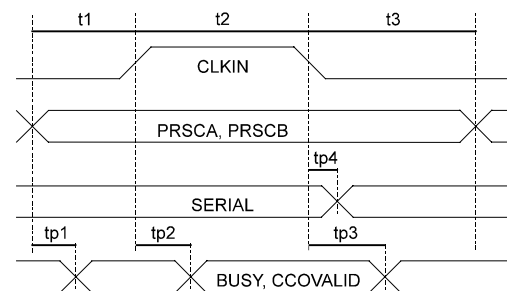


Figure 6. Timing definition

timing diagrams

conditions	t1 (ns)	t2 (ns)	t3 (ns)	tp1 (ns)	tp2 (ns)	tp3 (ns)	tp4 (ns)
$T_{amb.} = -10\text{ }^{\circ}\text{C}$, $V_{dd} = 5.5\text{ V}$				25	31	37	27
$T_{amb.} = 25\text{ }^{\circ}\text{C}$, $V_{dd} = 5.0\text{ V}$ (typical)	200	300	300	55	60	90	58
$T_{amb.} = 75\text{ }^{\circ}\text{C}$, $V_{dd} = 4.5\text{ V}$				110	232	191	121

Table 4. Timing definition for digital part ($C_{load} = 125\text{ pF}$, $f_{test} = 1.25\text{ MHz}$).

electrical specifications

rating	symbol	min.	max.	unit
supply voltage	VDD	- 0.5	13	V
I/O voltage	$V_{IN} \cdot V_{OUT}$	- 0.5	VDD + 0.5	V
I/O current	$I_{IN} \cdot I_{OUT}$	- 100	+ 100	mA
storage temperature ceramic package plastic package	T_{STG}	- 65 - 40	+ 150 + 125	$^{\circ}\text{C}$

Table 5. Absolute maximum ratings ($T_J = 25\text{ }^{\circ}\text{C}$, voltages referred to VSS unless otherwise specified).

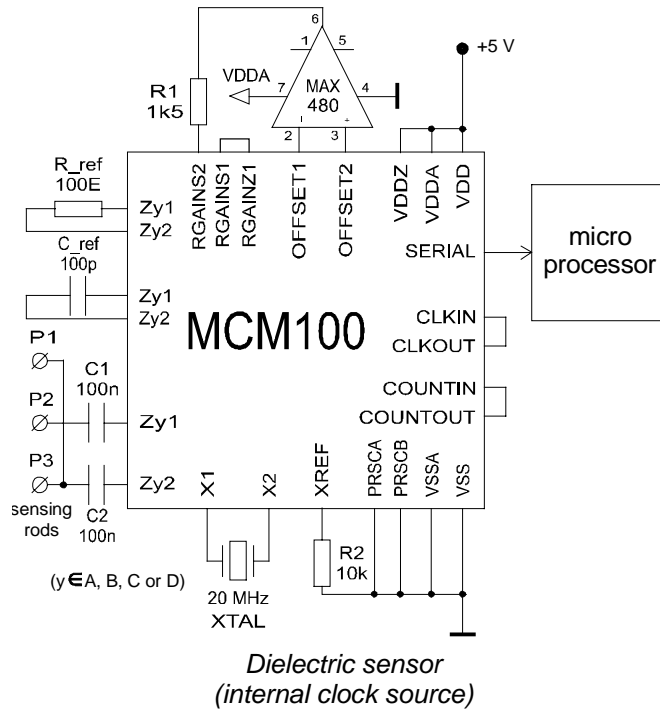
characteristics	symbol	min.	typ.	max.	unit
supply voltage	VDD	4.5	5.0	5.5	V
input voltage	V_{IN}	0		VDD	V
supply current	I_{supply}		35		mA
operating temperature commercial	T_{OPER}	0		+ 70	$^{\circ}\text{C}$

Table 6. Recommended operating conditions (voltages referred to VSS unless otherwise specified).

characteristics	symbol	min.	typ.	max.	unit
CMOS input voltage high level low level	V_{IH} V_{IL}	70% VDD -	- -	- 30% VDD	V
3-state output leakage $V_O = VDD$ $V_O = VSS$	$I_{OZ(H)}$ $I_{OZ(L)}$	- - 10	- -	10 -	μA
input current high level ($V_I = VDD$) standard pull-down low level ($V_I = 0\text{ V}$) standard pull-up	I_{IH} I_{IL}	- - - 10 - 100	- - - -	10 100 - -	μA
maximum admissible current per pin	I_{CC}		± 100	-	mA
maximum DC I/O current per pin to avoid latch-up	I_{CC}		± 100		mA
Electrostatic discharge protection	V_{ESD}	-	4000	-	V

Table 7. General DC characteristics.

application examples



mechanical data

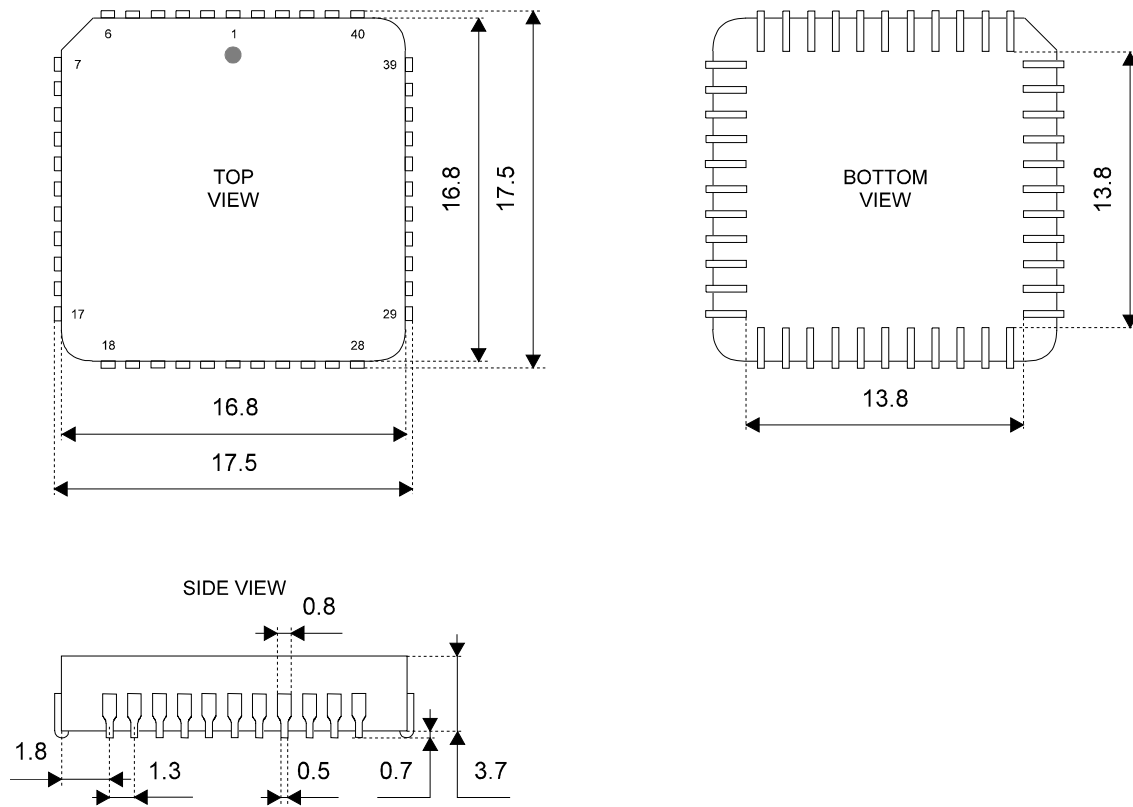


Figure 7. Mechanical data shown in a top view, a bottom view and a side view. All dimensions in mm.

APPLICATION NOTE

A NEW SENSOR FOR DIELECTRIC SOIL CHARACTERISATION

by Dr. Max A. Hilhorst

This application note is a reprint of chapter 3 in the phd-thesis: "Dielectric Characterisation of Soil", by dr. Max. A. Hilhorst, feb 1998, pp. 45-71. It is available as a publication nr. 98-01, ISBN 90-5406-162-6 of the DLO Institute of Agricultural and Environmental Engineering (IMAG-DLO), P.O. Box 43, NL-6700 AA Wageningen, The Netherlands.